AND8429/D

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Using ON Semiconductor's Serial EEPROMs in Shared Input/Output Configuration

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APPLICATION NOTE

ON Semiconductor's family of serial E^2PROMs utilizes 4 signals for the communication interface; Chip Select (CS) for device selection, Serial Clock (SK or CLK) for synchronizing serial data to and from the device, Data Input (DI) to input serial data to the device and Data Output (DO) to output serial data from the device. This interface can be reduced to 3 signals by sharing DI and DO as a common input/output signal. However, the following precautions should be taken to prevent problems due to DI/DO contention:

1) READ Instruction in Shared DI/DO Configuration:
(applies to 93C46, 93C56, 93C57, 93C66 and 93C86)

Data Output Pin (DO) remains in high impedance state while most of the READ instruction (i.e. start bit, opcode and address) is being input and offers no contention to the Data Input Pin (DI) driver in a shared DI/DO configuration (Figure 1). However, typically 50 ns after the rising edge of the serial clock shifts in the least significant bit of the address stream (A0), DO outputs the dummy '0' bit to flag the beginning of the output data stream. If A0 is a '1' and the DI driver has not been disabled by the time the '0' dummy bit becomes valid, a low impedance path between the system power supply and ground is created through the DI driver pullup and DO pulldown device (Figure 2).

Unless this condition causes excessive noise on the system power supply (which may in turn cause noisy or spurious signals to the device), the READ instruction will continue and complete normally since A0 is already shifted into the device.

To minimize potential problems during this low impedance condition, a current limiting resistor should be placed between the DI driver and the DO pin when in shared DI/DO configuration (Figure 3).

Alternatively, an open drain (or open collector) DI driver with pullup resistor could be used (Figure 3).

In either case, the clocking rate should be slow enough to ensure that the resistor can charge or discharge the shared DI/DO bus capacitance before the appropriate clock edge. For example, if the resistor used is 10 KΩ, and the bus capacitance is 100 pF, then a safe clock rate is calculated to be:

Clock Period (T) = 2 x 3RC
= 2 x 3 x 10 kΩ x 100 pF
= 6 μsec

Frequency (f) = 1 / T
= 167 KHz

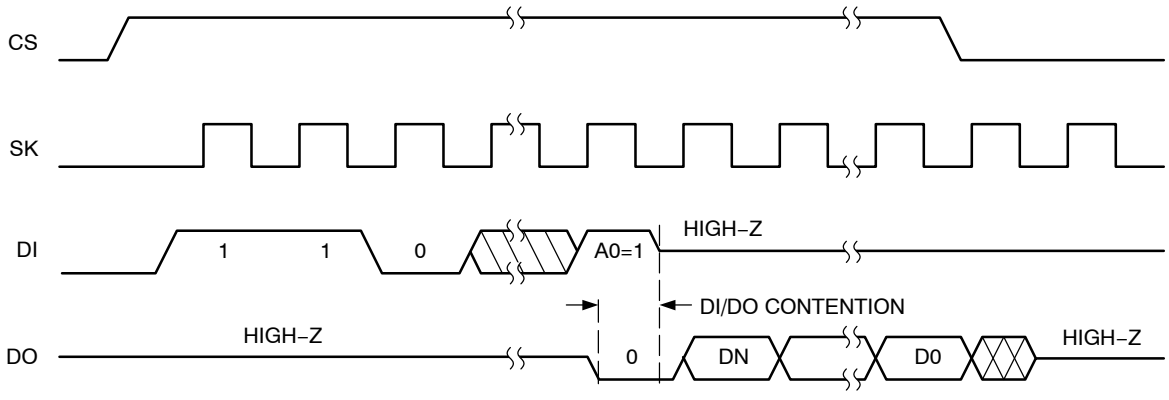

Figure 1. DI/DO Contention Timing During Read Cycle

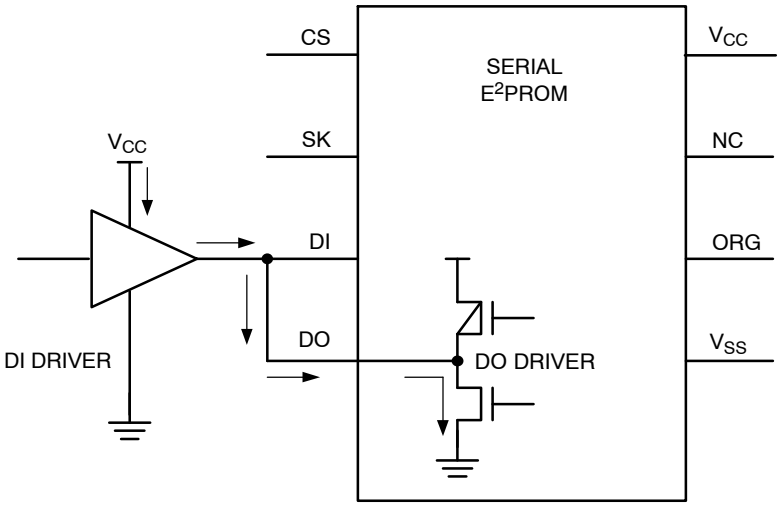

Figure 2. Current Path

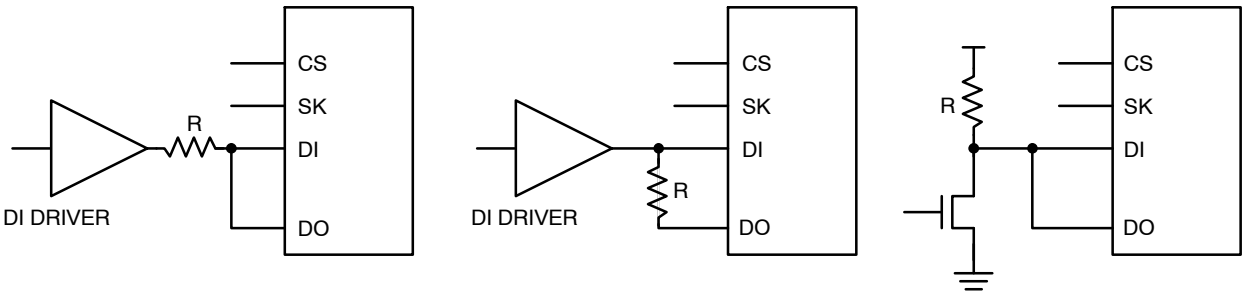

Figure 3. Possible Configurations to Minimize Problems Due to READ Contention

2) Programming Instructions in Shared DI/DO Configuration:

(93C46, 93C56, 93C57, 93C66 and 93C86 only)

All 3−Wire devices feature self−timed programming cycles. A programming status signal indicates whether the self−timed programming cycle is still in progress or has been completed. A ‘0’ status signal indicates that the device is still programming mode, while a ‘1’ status signal indicates that the programming cycle has been completed and the device is ready to receive the next instruction. This feature will allow a user to minimize the programming time (t_{EW}).

On the 93C46, 93C56, 93C57, 93C66 and 93C86 serial E^2PROMs, the programming status signal can be read on the DO pin by bringing CS high after initiating a programming cycle. In a 4−signal interface, after a programming cycle is complete, the status signal is reset to high impedance by the start bit of the next instruction (Figure 4).

In a shared DI/DO configuration, the ‘1’ status signal on DO can be clocked into the device as a start bit and reset the status signal before it can be read. This can interfere with the DI signal of the next instruction cycle. The following steps are recommended to avoid these conditions for a 3−signal interface (Figure 5):

1. The clock (SK) should be stopped after shifting in the programming instruction. This prevents the ‘1’ ready status from resetting the status signal before it can be read.
2. After reading the ‘1’ ready status, at least one clock pulse should be input to the device while the DI/DO signal is ‘1’ in order to reset the status signal.
3. CS should then be brought low to reset the instruction logic.

The next instruction can now be executed without any contention from the DO signal.

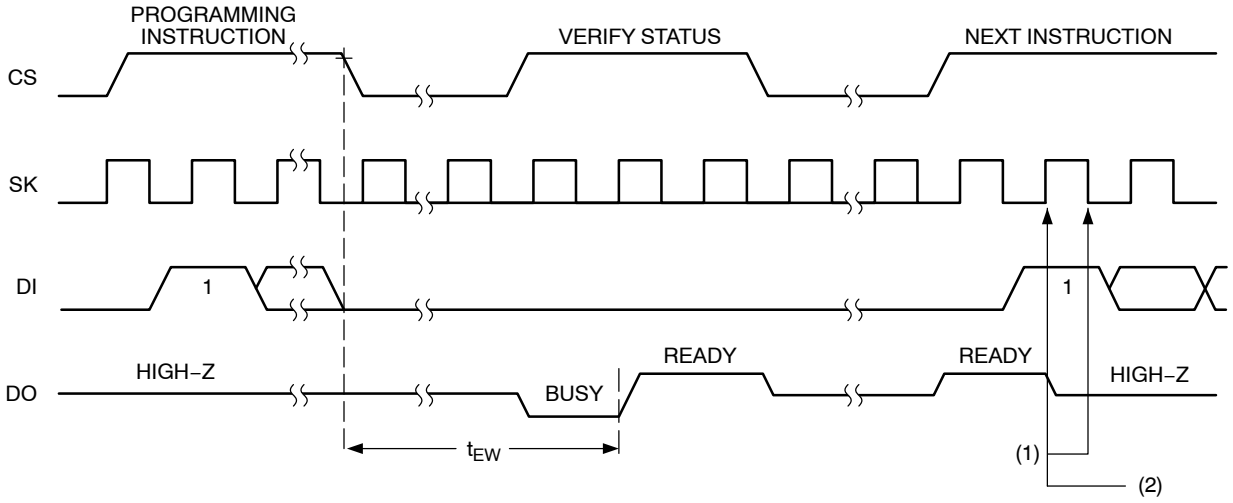

Figure 4. Programming Instruction and Status Reset with 4−Signal Interface

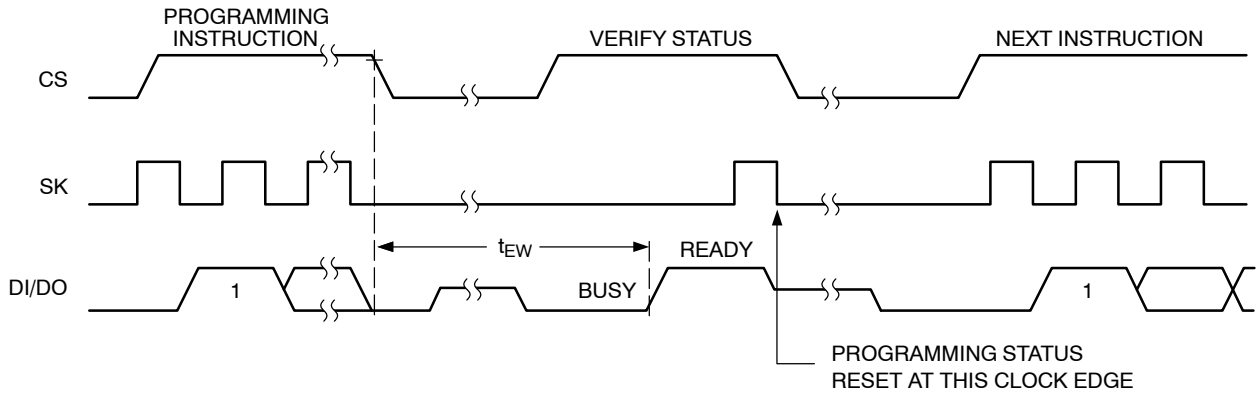

Figure 5. Programming Instruction and Status Reset with 3−Signal Interface

1. Programming status reset on falling clock edge (93C46).
2. Programming status reset on rising clock edge (93C46, 93C57, 93C66 and 93C86).

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